**Hardware Development Plan**

The following plan lays out the how our team will approach the Verilog Stopwatch project. The first section will cover the standards that apply to this project. The Second section covers how life cycle data will be tracked throughout the development cycle. The third and final section covers the different software and tools that will be used during this project.

1. Scope
2. Purpose:
3. Standards

The following documents will define the standards for which this project will uphold with regards to coding practices, requirements generation, and branching strategies.

* 1. [Coding Standards](https://lnttsgroup.sharepoint.com/sites/LTTS-Collins-FPGATraining/_layouts/15/Doc.aspx?sourcedoc=%7BD717F7B6-E49C-4A3D-8979-9C33B494EDD0%7D&file=Coding%20Standards.docx&action=default&mobileredirect=true&CT=1591630910639&OR=ItemsView).v1
  2. [Requirements Standards](https://lnttsgroup.sharepoint.com/sites/LTTS-Collins-FPGATraining/_layouts/15/Doc.aspx?sourcedoc=%7B9B8D3923-8CBC-4A8B-835B-5399245B6A96%7D&file=Requirements%20Standards.docx&action=default&mobileredirect=true&CT=1591630925910&OR=ItemsView).v1
  3. [Branching Strategy Standards](https://lnttsgroup.sharepoint.com/sites/LTTS-Collins-FPGATraining/_layouts/15/Doc.aspx?sourcedoc=%7B2C639C94-C1F3-44DD-9050-C09DAD3E4F11%7D&file=Branching%20strategy.docx&action=default&mobileredirect=true&CT=1591630951111&OR=ItemsView).v1

1. Hardware Life-Cycle Data

The following is how we will track the progress of our project. As the project evolves we will record our progress both in documentation and with life-cycle data.

* 1. Life-Cycle Tracking Metrics
     1. Number of git commits and new or edited lines of code shall be recorded at the end of stages 2, 3, and 4.
     2. Jira *Burndown Charts* and *Cumulative Flow Diagrams* shall be saved at the end of each sprint.
  2. Project Stages:
     1. Stage 0: Training & Planning, Deadline: 06/09
     2. Stage 1: Requirements Generation, Deadline: 06/11
        1. Generate Requirements
        2. Requirements Review/Sign-off
     3. Stage 2: Coding and Implementation, Deadline: 06/14
        1. Develop individual Modules
        2. Write generic testbench for the Module
        3. Review/Sign-off on source code and generic testbench
     4. Stage 3: Functional Verification, Deadline: 06/18
        1. Generate Traceable testcases
        2. Develop Self Reporting Testbench
        3. Review/Sign-off on final testbench
     5. Stage 4: FPGA Integration, Deadline: 06/19

1. Developments Environment

Below is a list of tools and how they will be utilized by our team during this project.

* 1. Requirements & Tools: Requirements are written in Excel according to the standards above and then signed off on using a checklist in Word.
  2. Design & Tools: Design and functionality specifications are written in word.
  3. Coding & Tools: Xilinx Vivado shall be used for developing, compiling, and testing our source code.
  4. Compiler/Linker: xsim shall be used when simulating source code.
  5. Hardware: Digilent Nexys A7 shall be used for FPGA integration.